PVP 20

Code: 20EC4501D

III B.Tech - I Semester – Regular Examinations - DECEMBER 2022

COMPUTER ARCHITECTURE & ORGANIZATION
(ELECTRONICS & COMMUNICATION ENGINEERING)

Duration: 3 hours Max. Marks: 70

Note: 1. This paper contains questions from 5 units of Syllabus. Each unit carries 14 marks and have an internal choice of Questions.
2. All parts of Question must be answered in one place.

BL – Blooms Level CO – Course Outcome

			BL	CO	Max. Marks
UNIT-I					
1	a)	Explain the register transfer and control functions with a neat block diagram.	L2	CO1	7 M
	b)	Analyze the working of arithmetic logic shift unit.	L3	CO2	7 M
OR					
2	a)	Illustrate the working of bus system for four register with a neat diagram.	L2	CO1	7 M
	b)	Make use of 4-bit adder-subtractor and with an example show the working of it.	L3	CO2	7 M
UNIT-II					
3	a)	Outline the control functions and microoperations used for basic computer.	L2	CO1	7 M
	b)	Explain instruction cycle for the basic computer with a neat flowchart.	L2	CO2	7 M
OR					

4	a)	Differentiate between hardwired control and micoprogrammed control.	L2	CO1	7 M
	b)	Explain the three instruction code formats with example.	L2	CO2	7 M
UNIT-III					
5	a)	Write three-address, two-address, one-address and zero-address instructions for X= (A+B) * (C+D).	L3	CO3	7 M
	b)	An instruction "ADD R1, A" is stored at memory location 4004. R1 is a processor register and A is a memory location with address 400. Each instruction is 32-bit long. What will be the values of PC, IR and MAR during execution of the instruction?	L3	CO3	7 M
OR					
6	a)	Explain straight line sequencing and branching with an example.	L3	CO3	7 M
	b)	Demonstrate zero, one, two and three address instruction formats with examples.	L3	CO3	7 M
UNIT-IV					
7	a)	Apply booth's algorithm to multiply two numbers 23(multiplicand) and -9(multiplier).	L3	CO2	7 M
	b)	Compare associative mapping and set-associative mapping with neat diagrams.	L4	CO4	7 M
OR					
8	a)	Explain the addition and subtraction with signed 2-s complement data. Give examples for each.	L3	CO2	7 M

	b)	A block set associative cache consists of a total of 64 blocks divided into 4-block sets. The main memory contains 4096 blocks each of 128 words. i. How many bits are there in main memory address? ii. How many bits are there in each of the TAG, SET and WORD fields?	L4	CO4	7 M
UNIT-V					
9	a)	Explain how I/O devices should be organized in a priority structure.	L2	CO1	7 M
	b)	Analyze the operation of the instruction pipeline with a timing diagram of an instruction pipeline in the presence of a branch instruction encountered at instruction I3.	L4	CO4	7 M
OR					
10	a)	Compare and contrast software and hardware priority interrupts.	L2	CO1	7 M
	b)	Explain in detail vector processing.	L4	CO4	7 M